

FIG. 1A

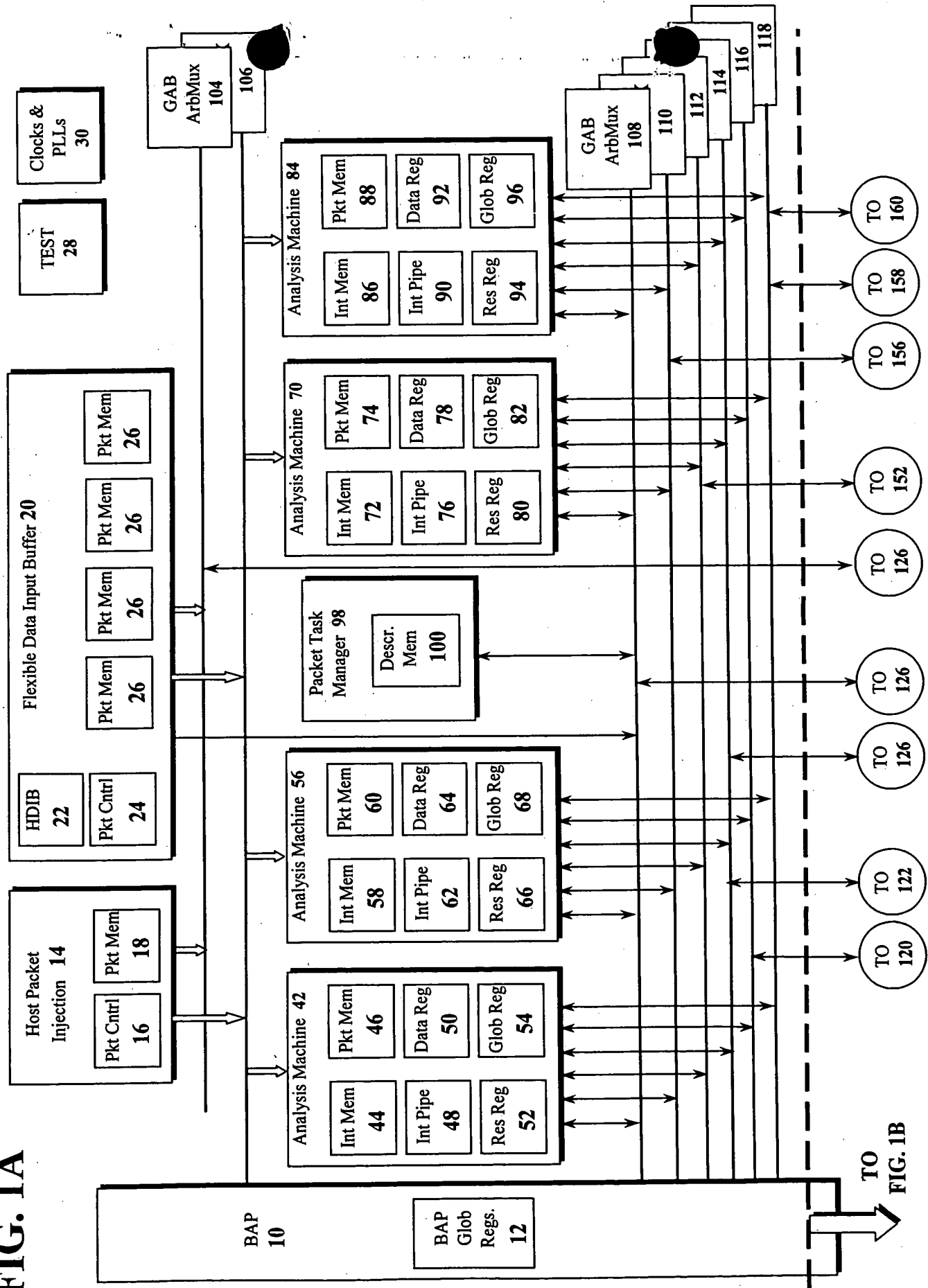
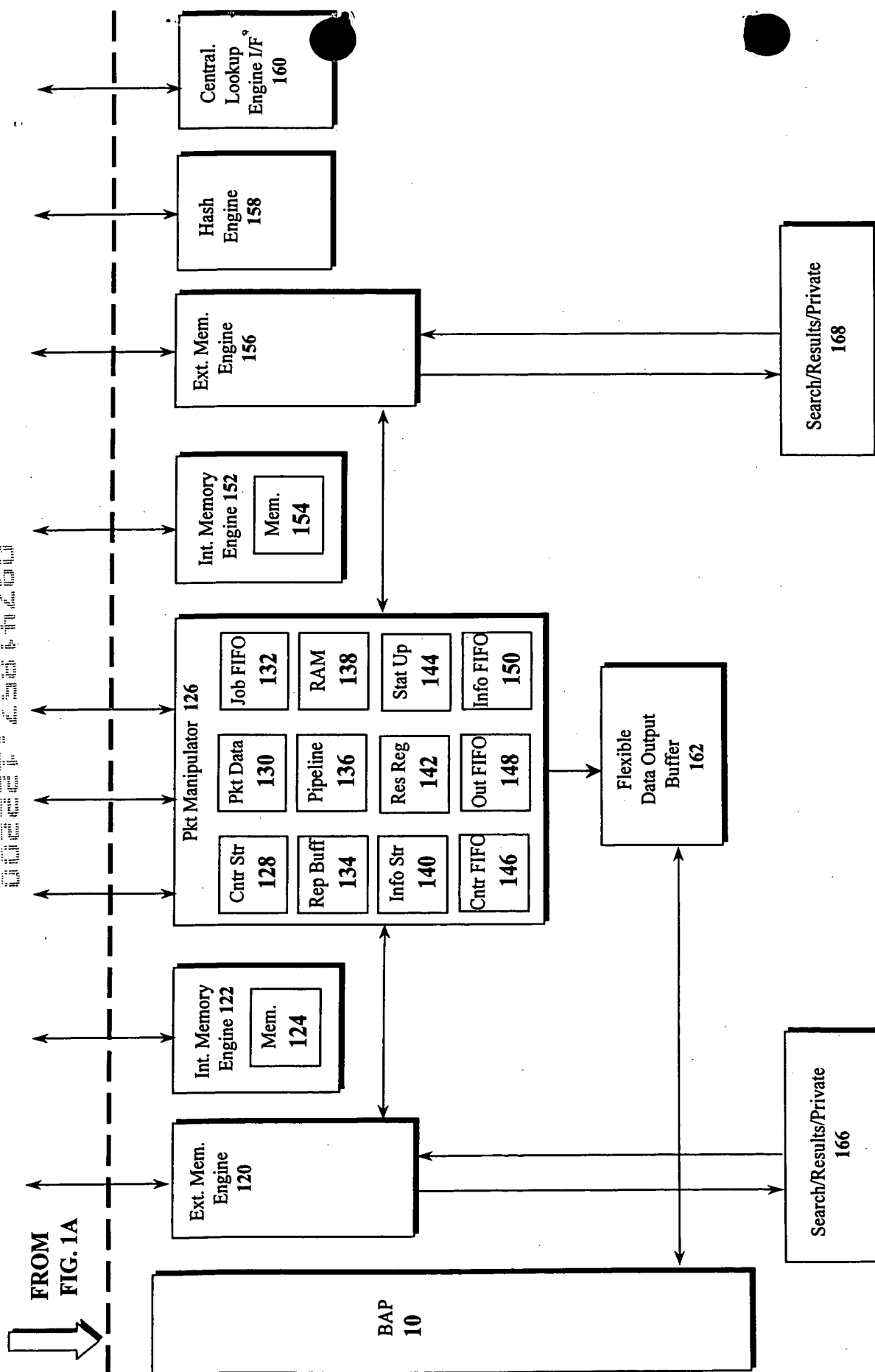


FIG. 1B

[illegible]

**FIG. 1B**

The diagram illustrates the G.2 system architecture, which is a parallel processing system. It features a central Host I/F (200) connected to four parallel processing channels (RSP2\_0, RSP2\_1, RSP2\_2, RSP2\_3). Each channel contains a CTGAB (202), a GAB ARB/MUX (240), a GAB ARB/MUX (242), a GAB ARB/MUX (244), and a GAB ARB/MUX (246). The channels are interconnected via a central bus (210, 212, 214, 216). The system also includes an External Memory Engine (220), Search Memory (230), and a Clue Clk (200Mhz).

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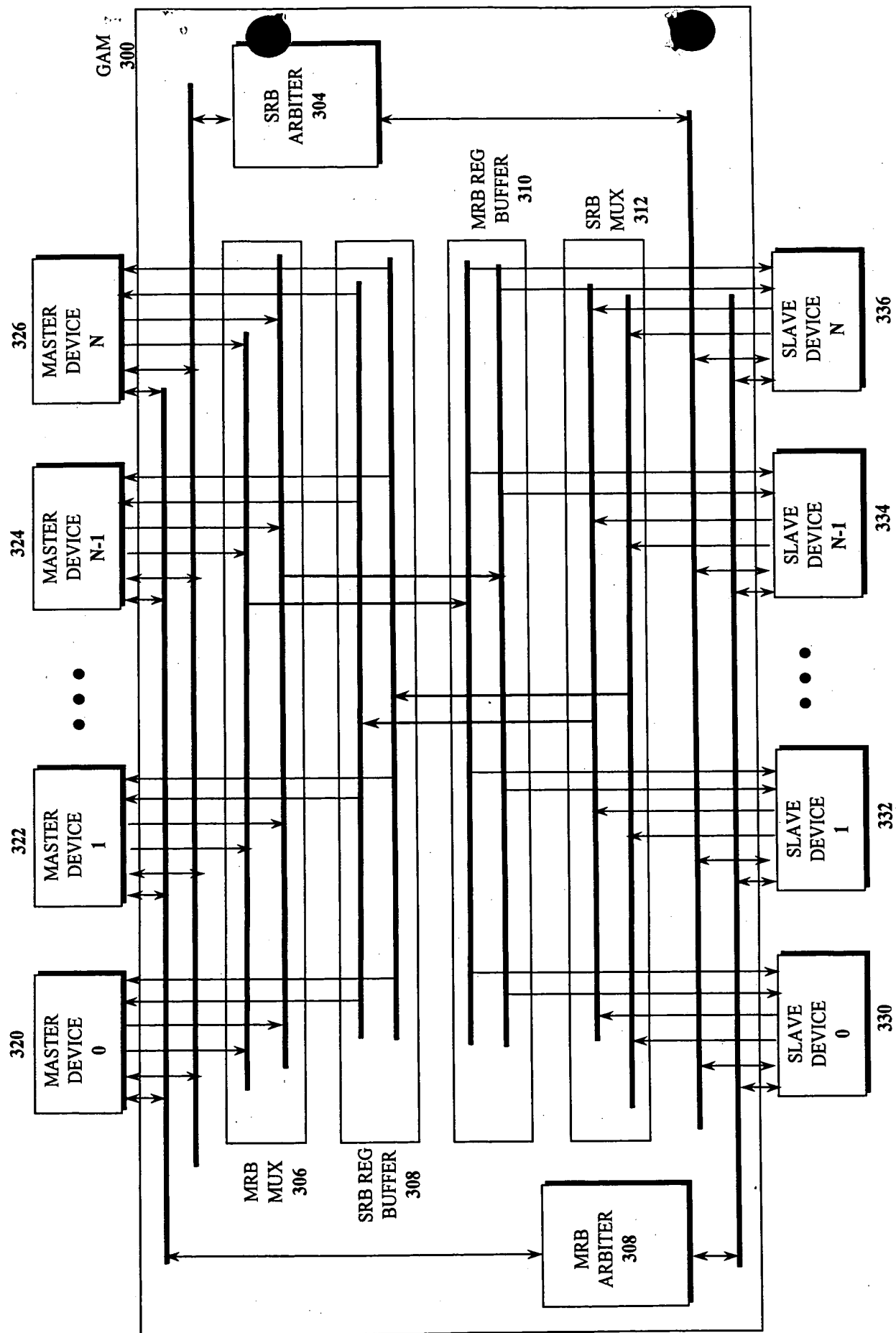


FIG. 3